Fig.1

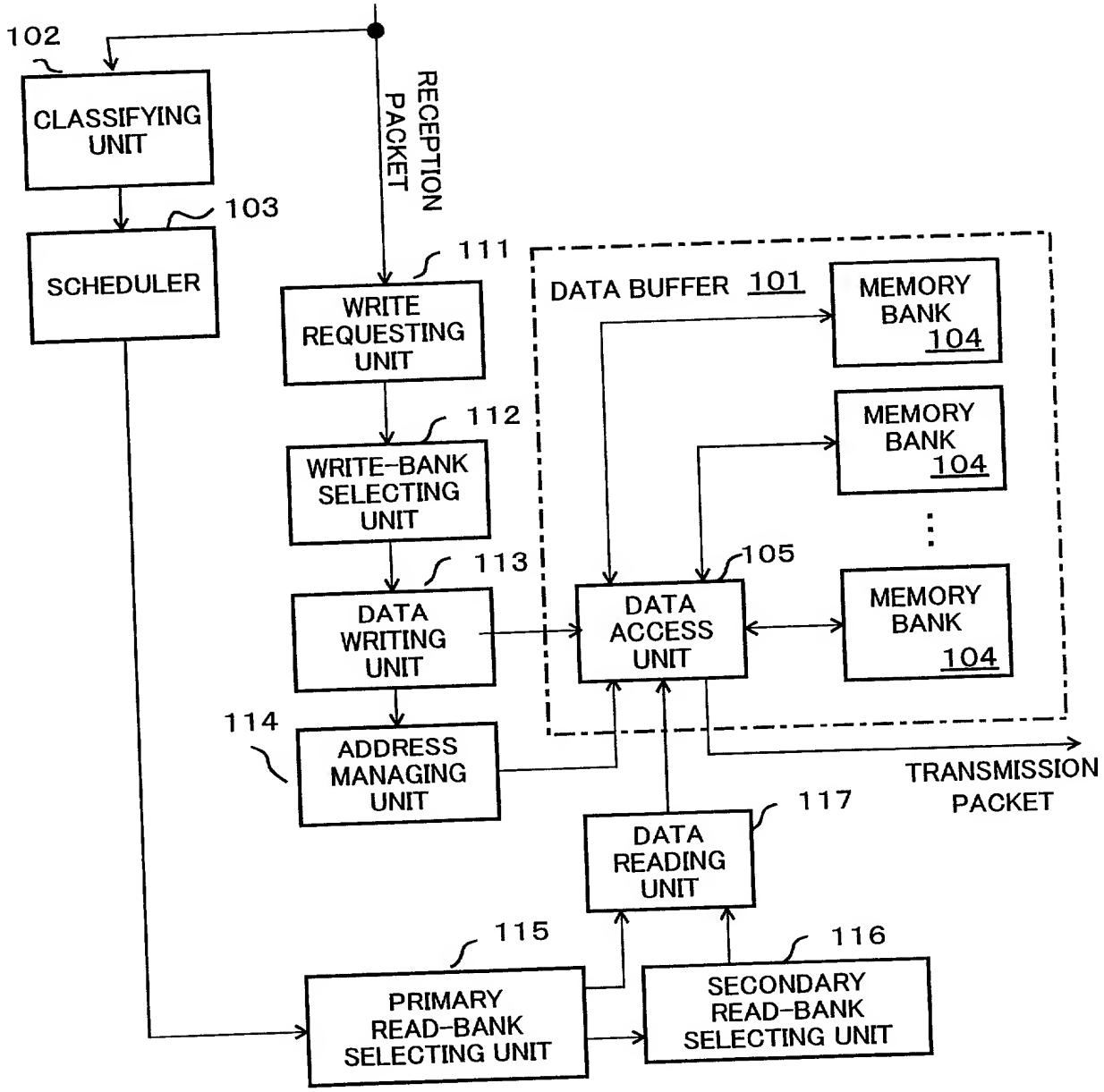

102
CLASSIFYING UNIT
103
SCHEDULER
RECEPTION PACKET
111
WRITE REQUESTING UNIT
112
WRITE-BANK SELECTING UNIT
113
DATA WRITING UNIT
114
ADDRESS MANAGING UNIT
DATA BUFFER 101
MEMORY BANK 104
MEMORY BANK 104
MEMORY BANK 104
105
DATA ACCESS UNIT
TRANSMISSION PACKET
117
DATA READING UNIT
115
PRIMARY READ-BANK SELECTING UNIT
116
SECONDARY READ-BANK SELECTING UNIT

Fig.2

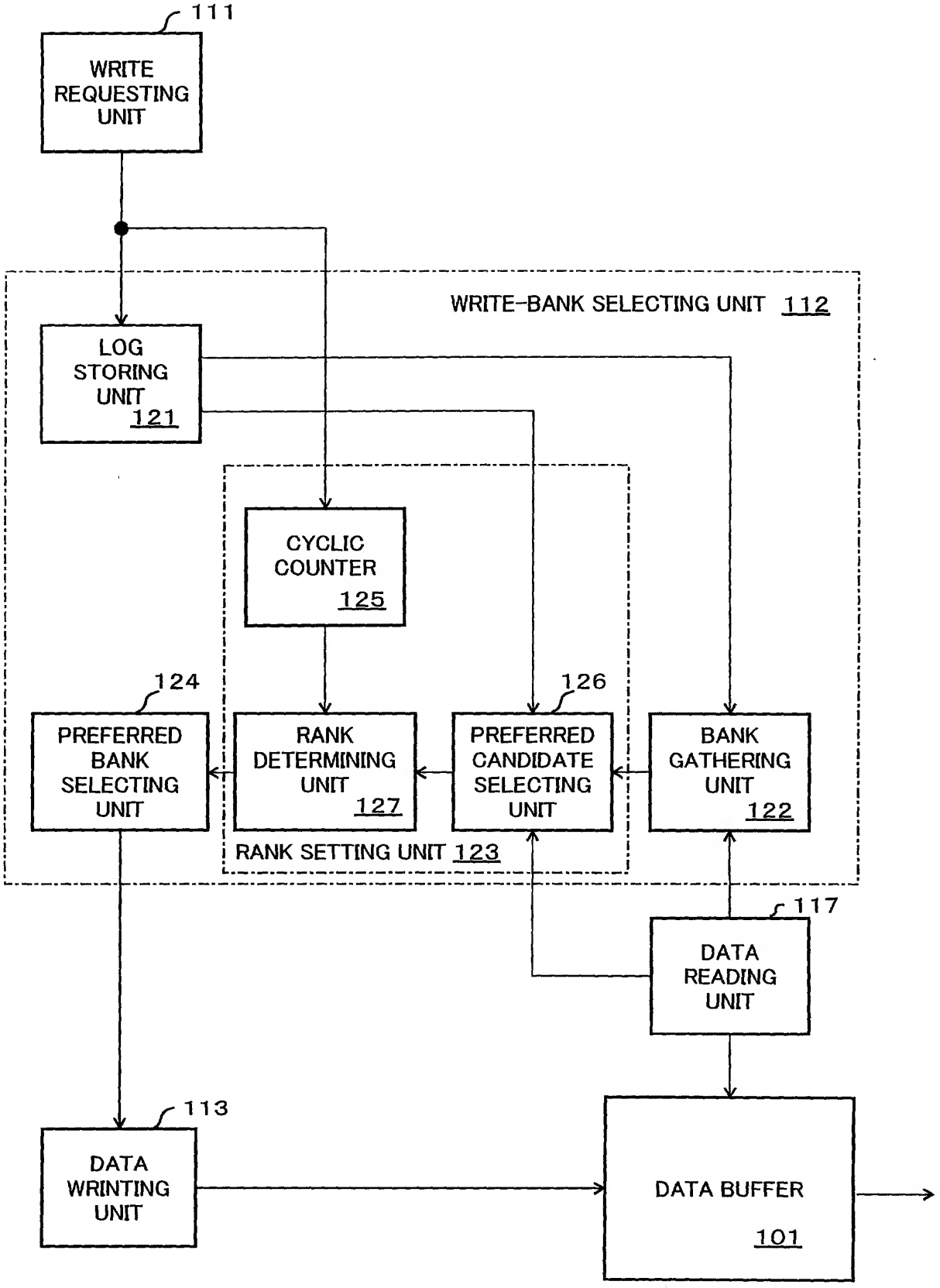

111
WRITE REQUESTING UNIT
WRITE-BANK SELECTING UNIT 112
LOG STORING UNIT 121
CYCLIC COUNTER 125
124
126
PREFERRED BANK SELECTING UNIT
RANK DETERMINING UNIT 127
PREFERRED CANDIDATE SELECTING UNIT
BANK GATHERING UNIT 122
RANK SETTING UNIT 123
117
DATA READING UNIT
113
DATA WRINTING UNIT
DATA BUFFER 101

Fig.3

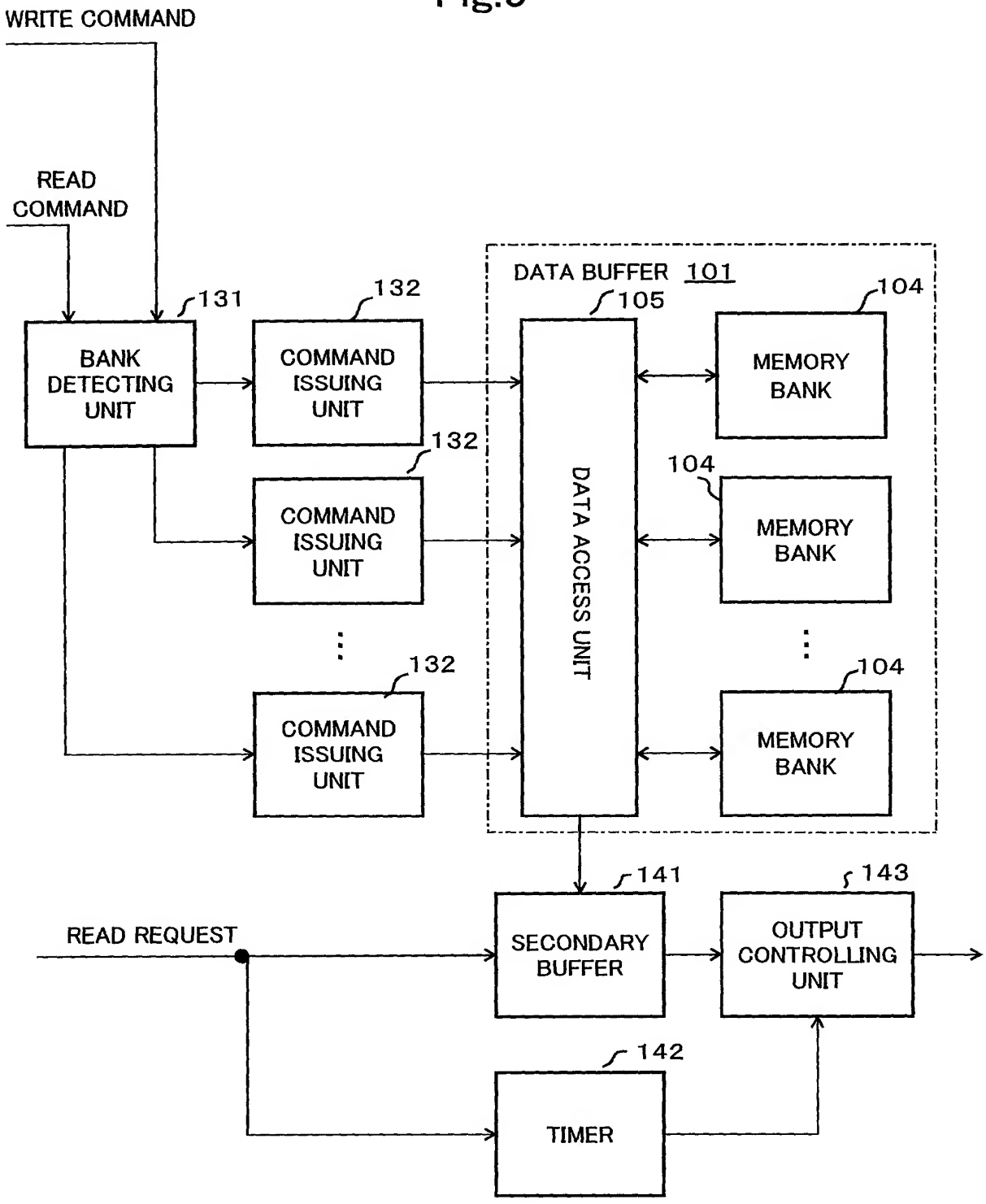

WRITE COMMAND
READ COMMAND
131
BANK DETECTING UNIT
132
COMMAND ISSUING UNIT
132
COMMAND ISSUING UNIT
132
COMMAND ISSUING UNIT
DATA BUFFER 101
105
DATA ACCESS UNIT
104
MEMORY BANK
104
MEMORY BANK
104
MEMORY BANK
141
SECONDARY BUFFER
143
OUTPUT CONTROLLING UNIT
READ REQUEST
142
TIMER

Fig.4

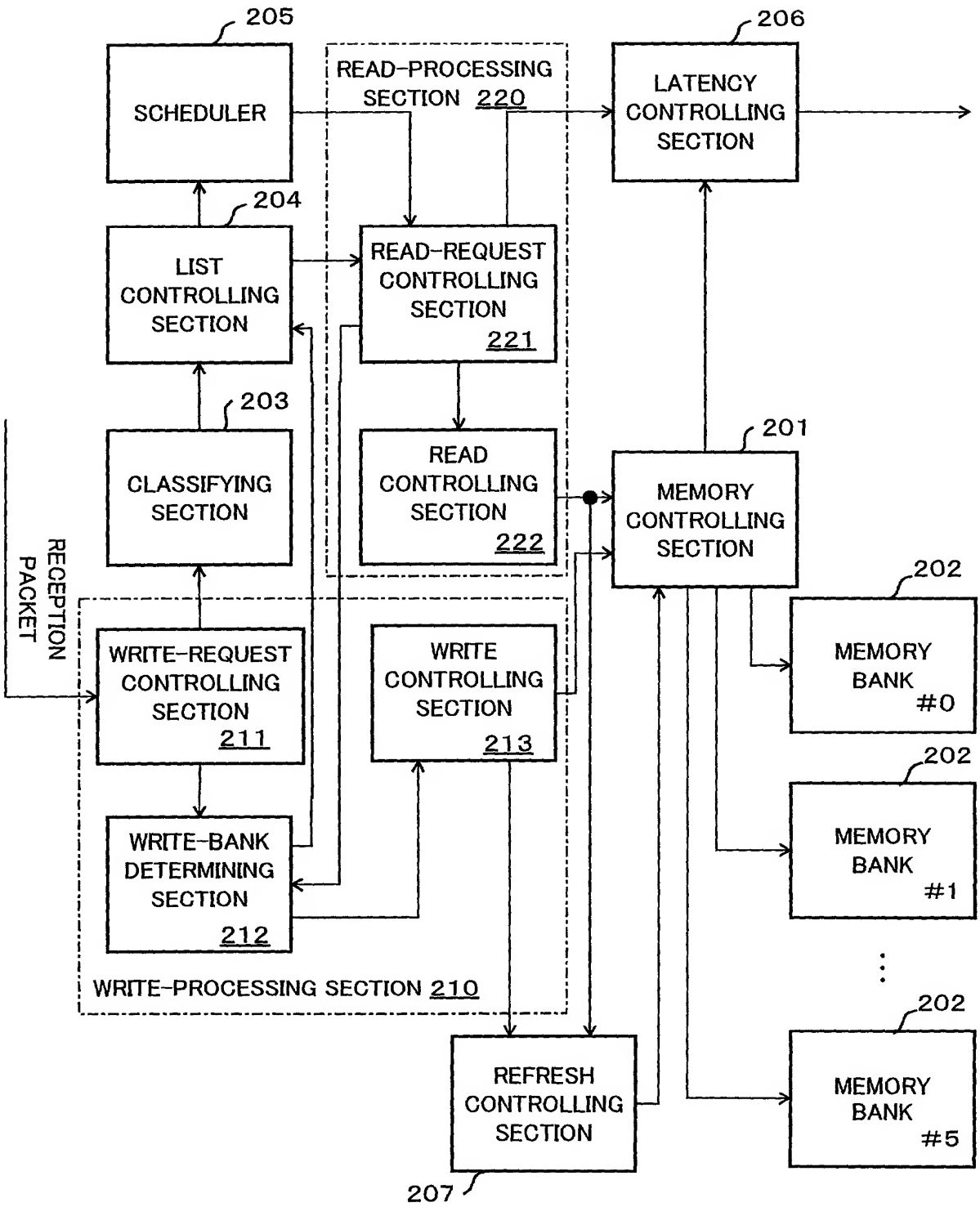

205
SCHEDULER
READ-PROCESSING SECTION 220
206
LATENCY CONTROLLING SECTION
204
LIST CONTROLLING SECTION
READ-REQUEST CONTROLLING SECTION 221
203
CLASSIFYING SECTION
READ CONTROLLING SECTION 222
201
MEMORY CONTROLLING SECTION
RECEPTION PACKET
WRITE-REQUEST CONTROLLING SECTION 211
WRITE CONTROLLING SECTION 213
202
MEMORY BANK #0
202
MEMORY BANK #1
WRITE-BANK DETERMINING SECTION 212
WRITE-PROCESSING SECTION 210
202
MEMORY BANK #5
REFRESH CONTROLLING SECTION
207

Fig.5

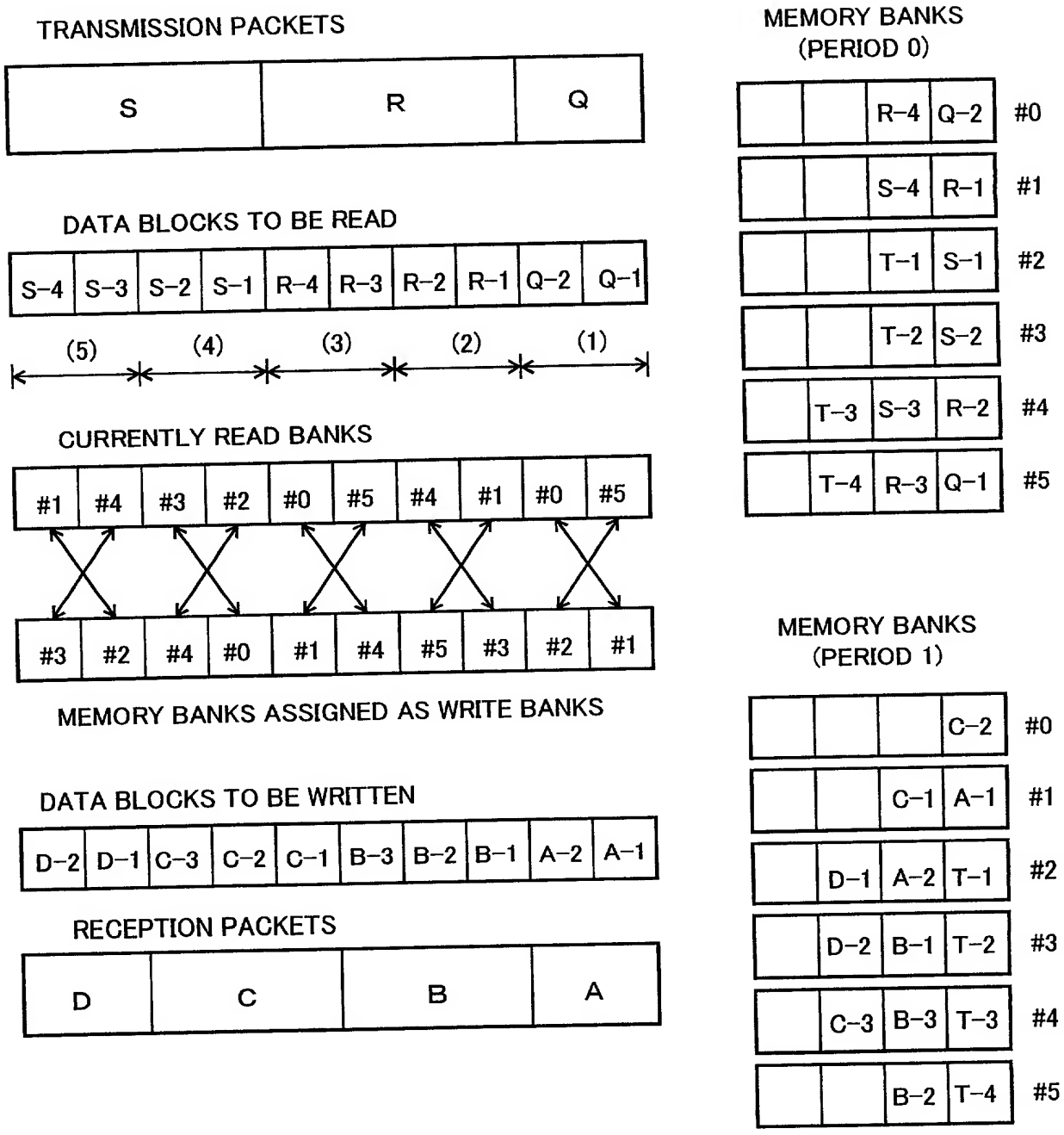

TRANSMISSION PACKETS
S
R
Q
DATA BLOCKS TO BE READ
S-4
S-3
S-2
S-1
R-4
R-3
R-2
R-1
Q-2
Q-1
(5)
(4)
(3)
(2)
(1)
CURRENTLY READ BANKS
#1
#4
#3
#2
#0
#5
#4
#1
#0
#5
#3
#2
#4
#0
#1
#4
#5
#3
#2
#1
MEMORY BANKS ASSIGNED AS WRITE BANKS
DATA BLOCKS TO BE WRITTEN
D-2
D-1
C-3
C-2
C-1
B-3
B-2
B-1
A-2
A-1
RECEPTION PACKETS
D
C
B
A
MEMORY BANKS
(PERIOD 0)
R-4
Q-2
#0
S-4
R-1
#1
T-1
S-1
#2
T-2
S-2
#3
T-3
S-3
R-2
#4
T-4
R-3
Q-1
#5
MEMORY BANKS
(PERIOD 1)
C-2
#0
C-1
A-1
#1
D-1
A-2
T-1
#2
D-2
B-1
T-2
#3
C-3
B-3
T-3
#4
B-2
T-4
#5

Fig.6

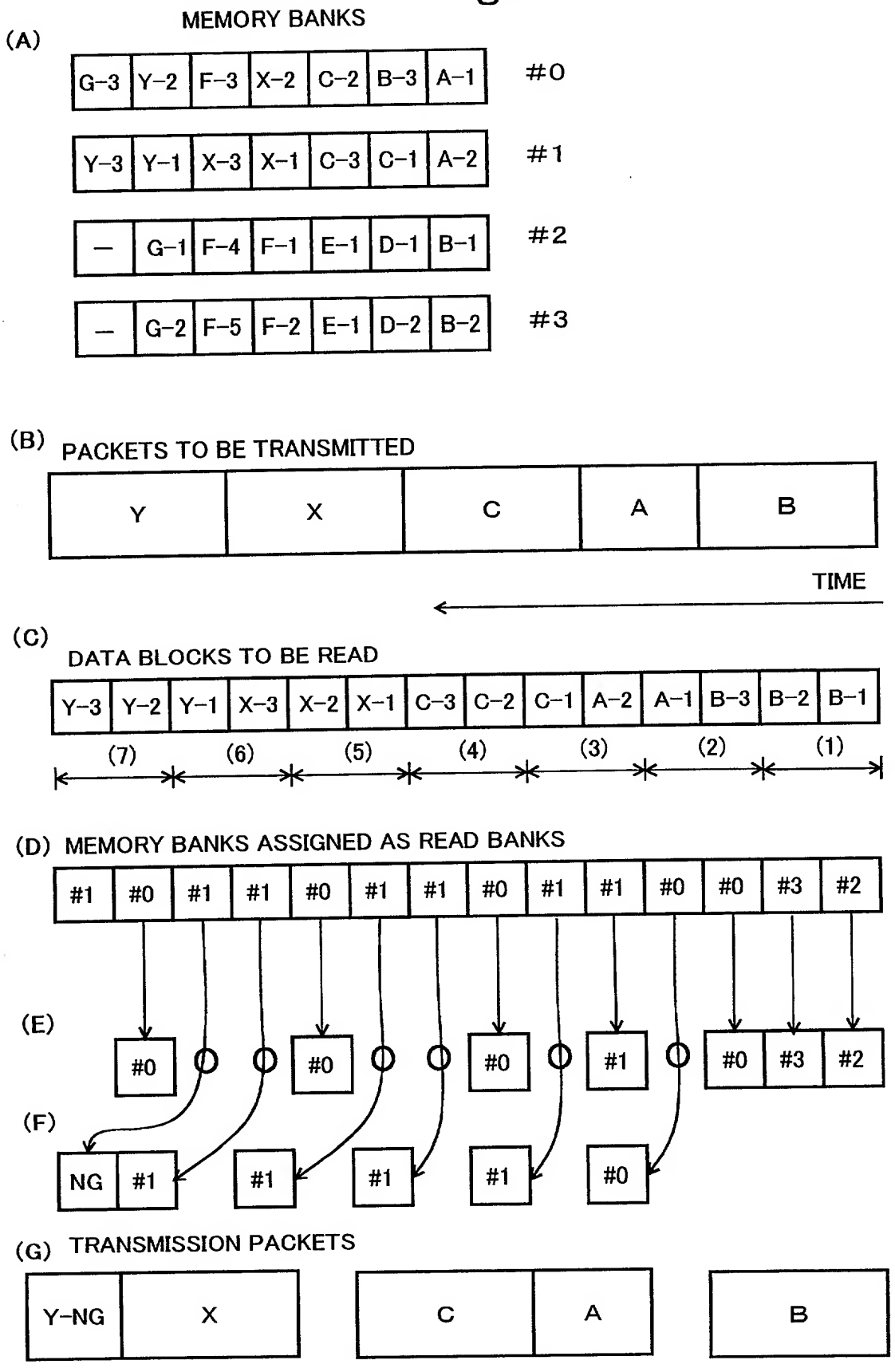

(A)
MEMORY BANKS
G-3 Y-2 F-3 X-2 C-2 B-3 A-1 #0
Y-3 Y-1 X-3 X-1 C-3 C-1 A-2 #1
— G-1 F-4 F-1 E-1 D-1 B-1 #2
— G-2 F-5 F-2 E-1 D-2 B-2 #3
(B) PACKETS TO BE TRANSMITTED
Y X C A B
TIME
(C)
DATA BLOCKS TO BE READ
Y-3 Y-2 Y-1 X-3 X-2 X-1 C-3 C-2 C-1 A-2 A-1 B-3 B-2 B-1
(7) (6) (5) (4) (3) (2) (1)
(D) MEMORY BANKS ASSIGNED AS READ BANKS
#1 #0 #1 #1 #0 #1 #1 #0 #1 #1 #0 #0 #3 #2
(E)
#0 #0 #0 #1 #0 #3 #2
(F)
NG #1 #1 #1 #1 #0
(G) TRANSMISSION PACKETS
Y-NG X C A B

Fig.7

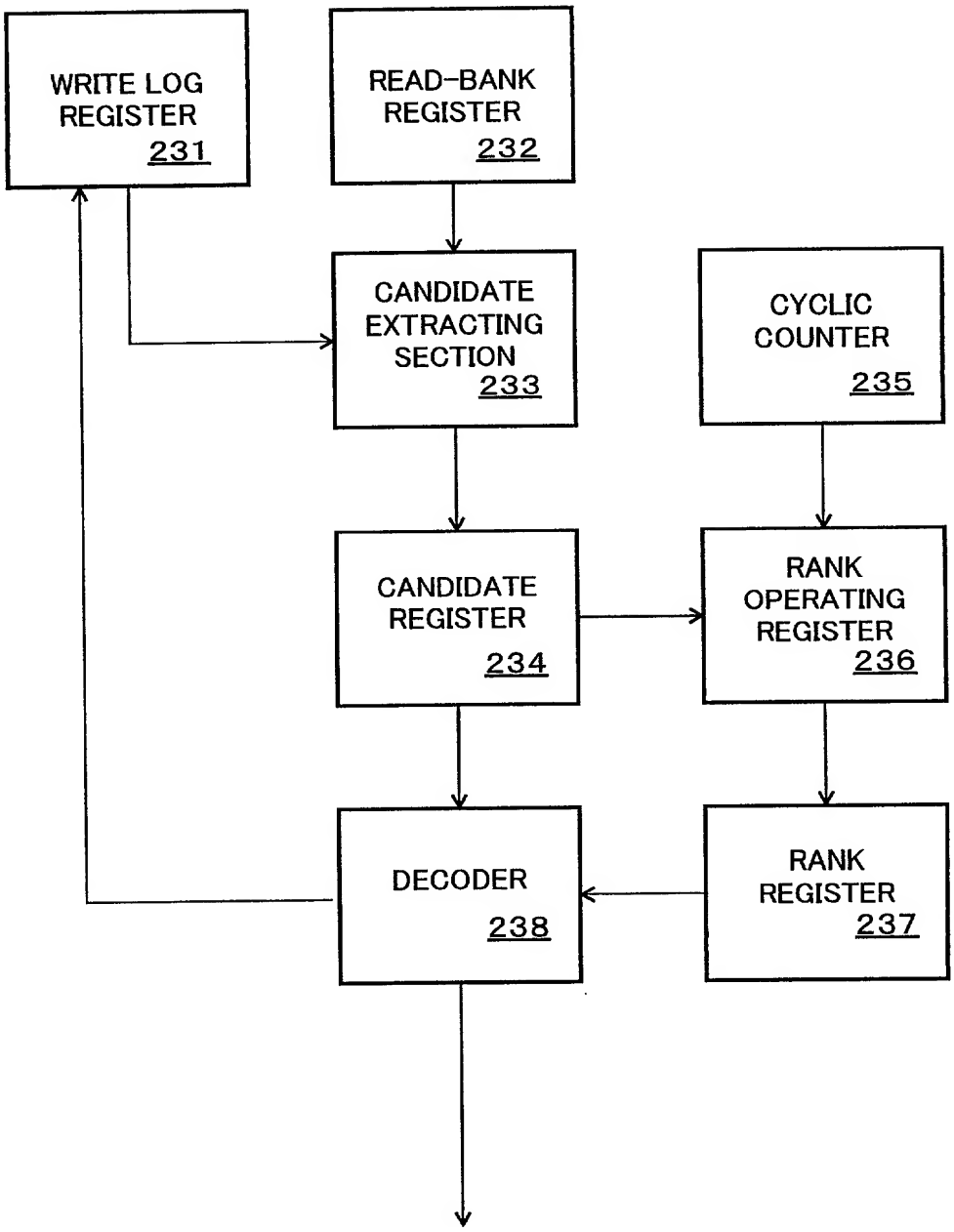
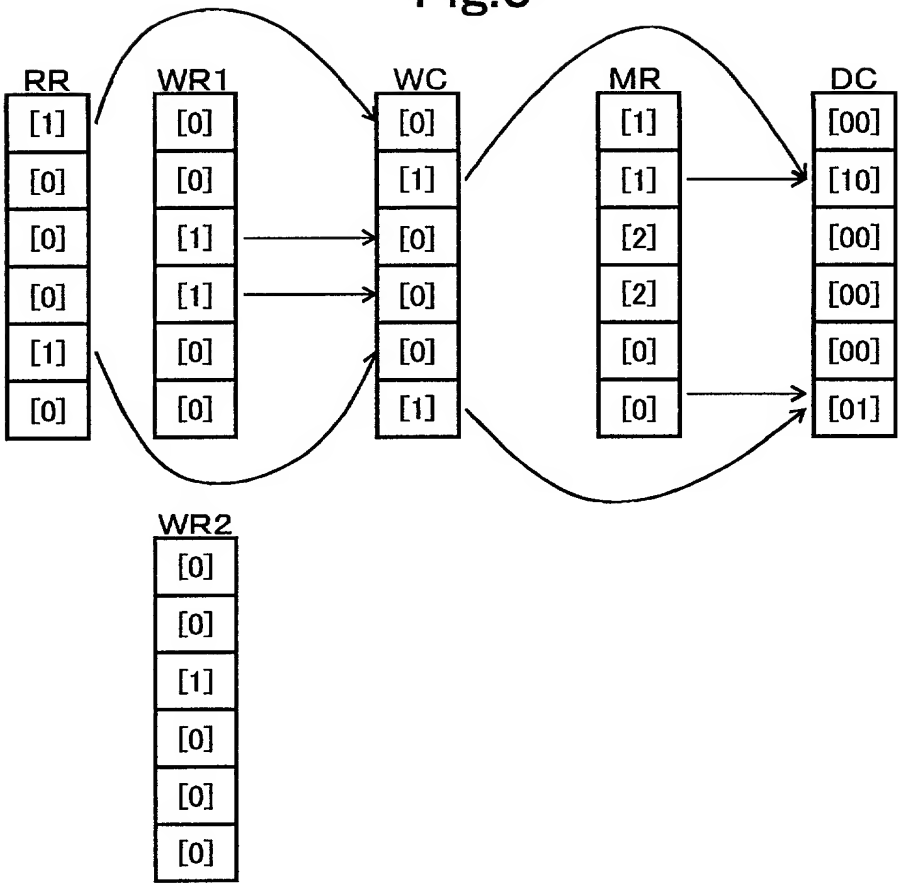

WRITE LOG REGISTER 231
READ-BANK REGISTER 232
CANDIDATE EXTRACTING SECTION 233
CYCLIC COUNTER 235
CANDIDATE REGISTER 234
RANK OPERATING REGISTER 236
DECODER 238
RANK REGISTER 237

Fig.8

(A)


RR
[1]
[0]
[0]
[0]
[1]
[0]
WR1
[0]
[0]
[1]
[1]
[0]
[0]
WC
[0]
[1]
[0]
[0]
[0]
[1]
MR
[1]
[1]
[2]
[2]
[0]
[0]
DC
[00]
[10]
[00]
[00]
[00]
[01]
WR2
[0]
[0]
[1]
[0]
[0]
[0]

(B)

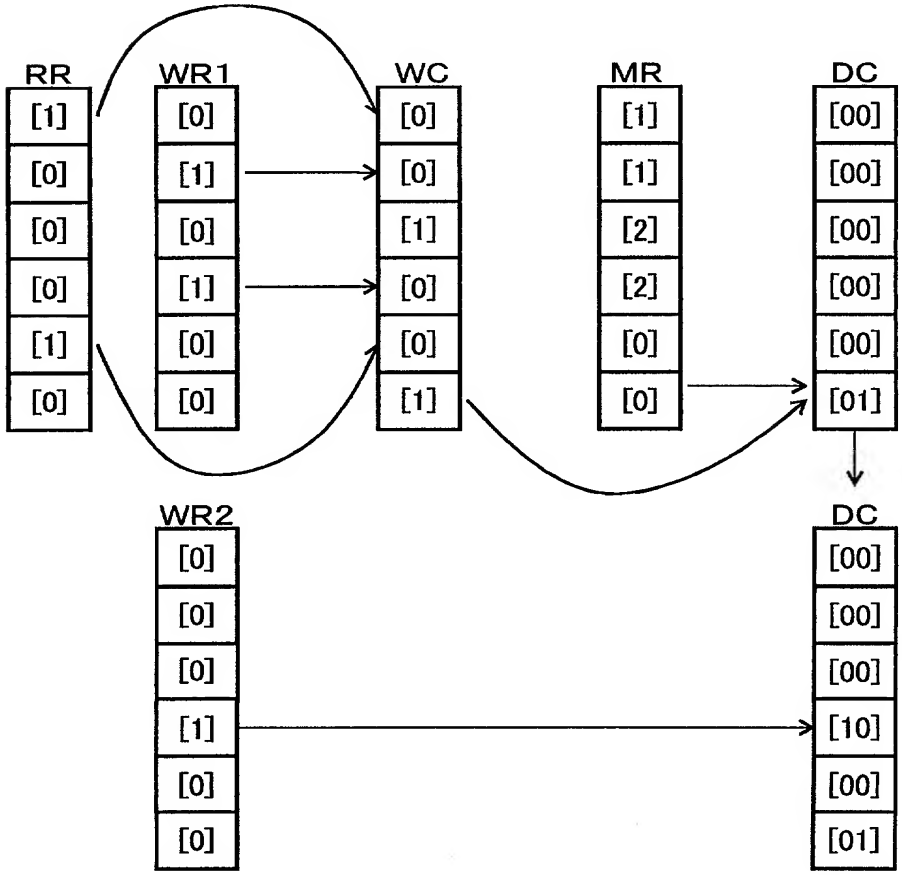

RR
[1]
[0]
[0]
[0]
[1]
[0]
WR1
[0]
[1]
[0]
[1]
[0]
[0]
WC
[0]
[0]
[1]
[0]
[0]
[1]
MR
[1]
[1]
[2]
[2]
[0]
[0]
DC
[00]
[00]
[00]
[00]
[00]
[01]
WR2
[0]
[0]
[0]
[1]
[0]
[0]
DC
[00]
[00]
[00]
[10]
[00]
[01]

Fig.9

	WC	P0		P1		P2		P3		P4		P5	
#0	[0]	0	0	Σ1-5	2	Σ2-5	1	Σ3-5	1	Σ4-5	1	Σ5	1
#1	[1]	Σ0	0	0	0	Σ2-0	1	Σ3-0	1	Σ4-0	1	Σ5-0	1
#2	[0]	Σ0-1	1	Σ1	1	0	0	Σ3-1	2	Σ4-1	2	Σ5-1	2
#3	[0]	Σ0-2	1	Σ1-2	1	Σ2	0	0	0	Σ4-2	2	Σ5-2	2
#4	[0]	Σ0-3	1	Σ1-3	1	Σ2-3	0	Σ3	0	0	0	Σ5-3	2
#5	[1]	Σ0-4	1	Σ1-4	1	Σ2-4	0	Σ3-4	0	Σ4	0	0	0

Fig.10

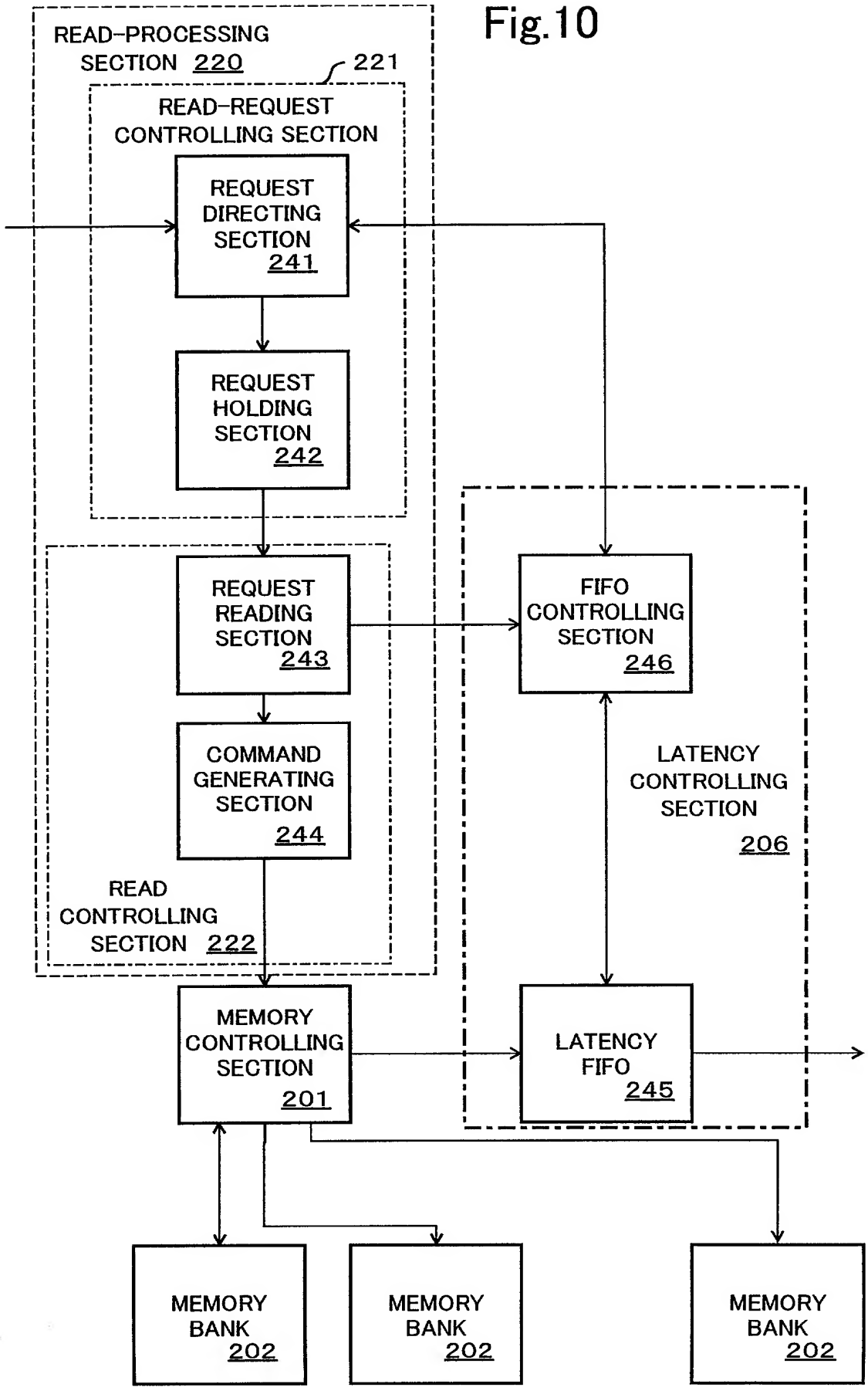

READ-PROCESSING SECTION 220
221
READ-REQUEST CONTROLLING SECTION
REQUEST DIRECTING SECTION 241
REQUEST HOLDING SECTION 242
REQUEST READING SECTION 243
COMMAND GENERATING SECTION 244
READ CONTROLLING SECTION 222
FIFO CONTROLLING SECTION 246
LATENCY CONTROLLING SECTION 206
MEMORY CONTROLLING SECTION 201
LATENCY FIFO 245
MEMORY BANK 202
MEMORY BANK 202
MEMORY BANK 202

Fig.11

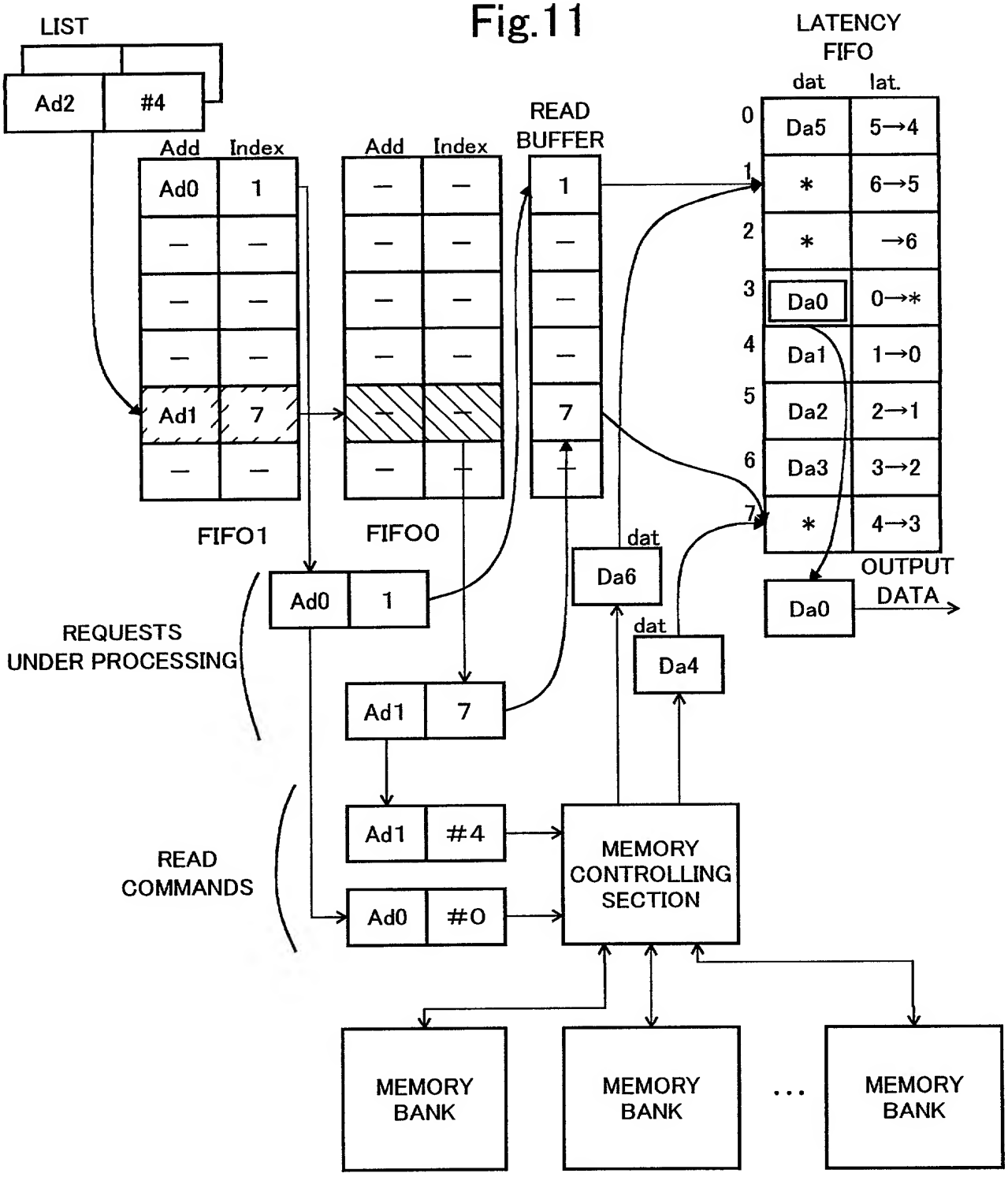

LIST
Ad2
#4
Add
Index
Ad0
1
Ad1
7
FIFO1
FIFO0
READ BUFFER
LATENCY FIFO
dat
lat.
Da5
5→4
*
6→5
→6
Da0
0→*
Da1
1→0
Da2
2→1
Da3
3→2
4→3
OUTPUT DATA
Da6
Da4
REQUESTS UNDER PROCESSING
READ COMMANDS
#4
#0
MEMORY CONTROLLING SECTION
MEMORY BANK
...

Fig.12

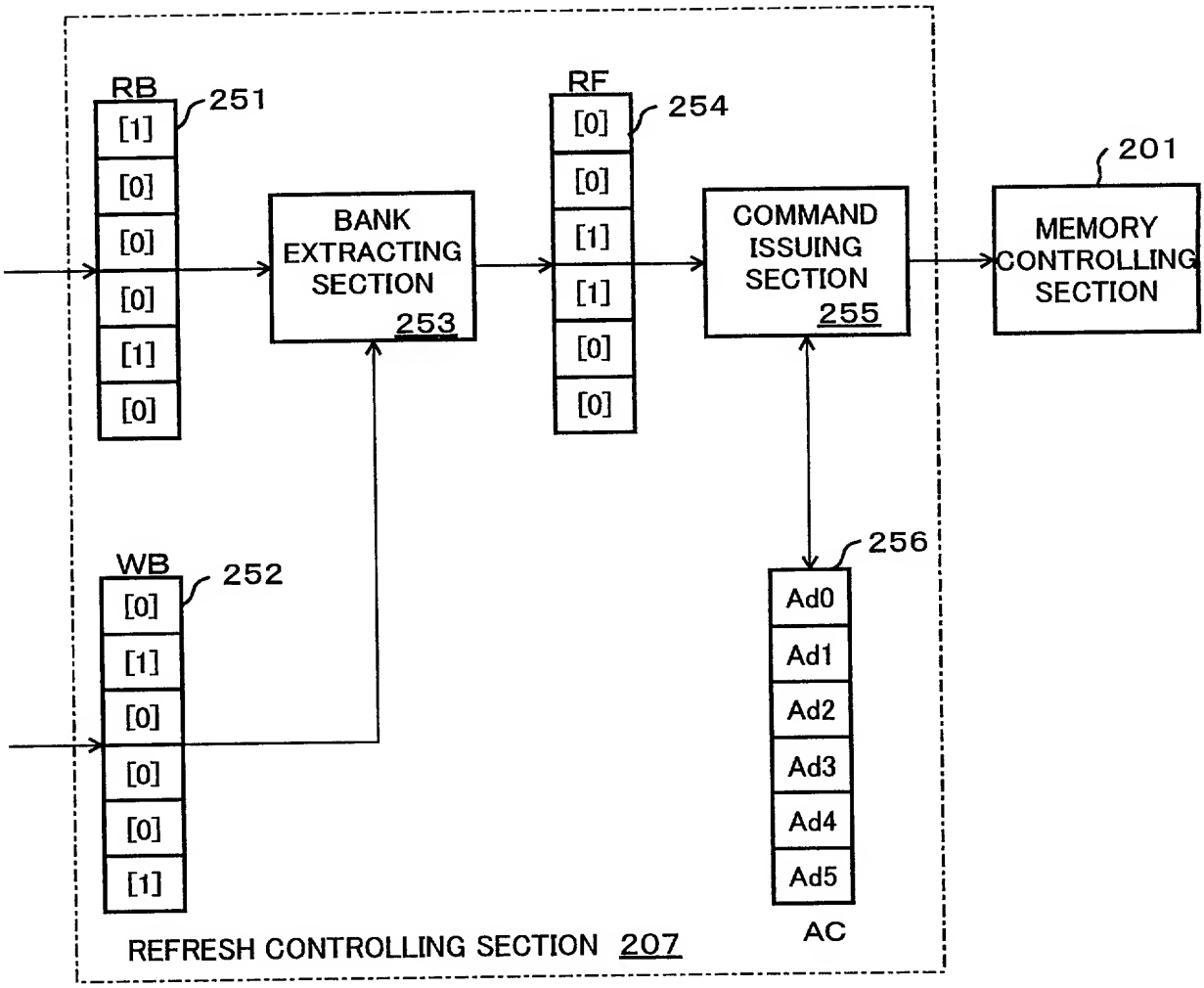

RB
251
[1]
[0]
[0]
[0]
[1]
[0]
BANK EXTRACTING SECTION
253
RF
254
[0]
[0]
[1]
[1]
[0]
[0]
COMMAND ISSUING SECTION
255
201
MEMORY CONTROLLING SECTION
WB
252
[0]
[1]
[0]
[0]
[0]
[1]
256
Ad0
Ad1
Ad2
Ad3
Ad4
Ad5
AC
REFRESH CONTROLLING SECTION 207

Fig.13 PRIOR ART

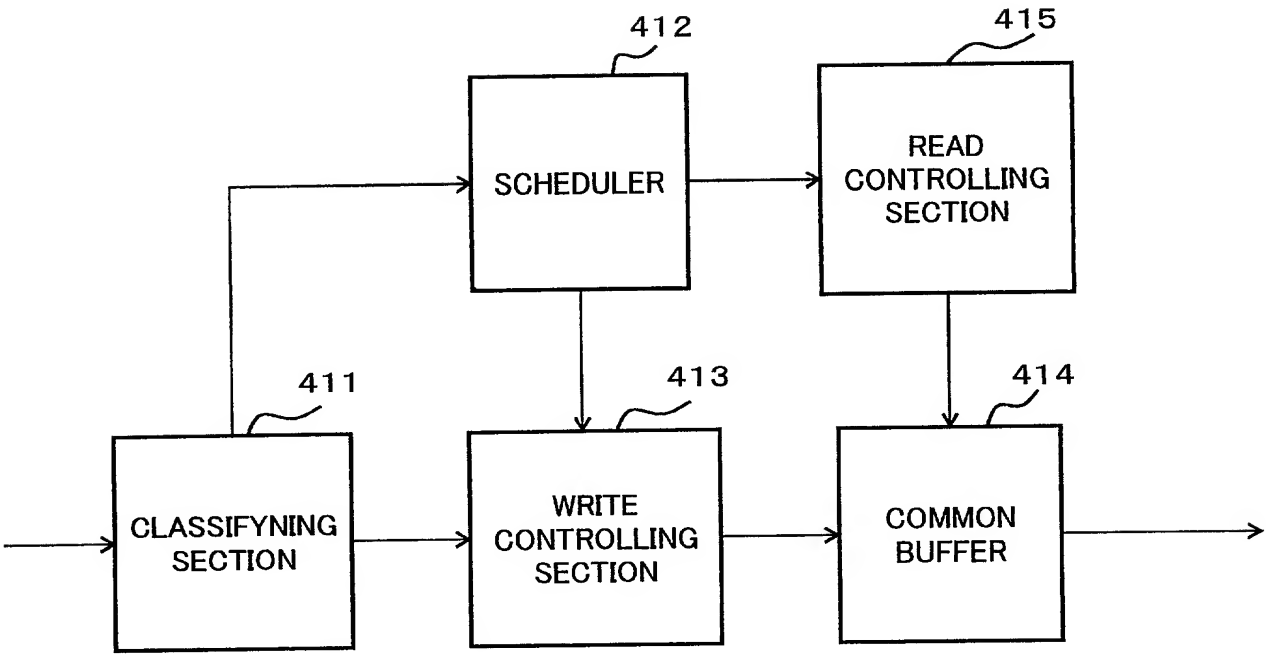


Fig.14 PRIOR ART